74HC75

Quad bistable transparant latch

Rev. 03 — 12 November 2004 **Product data sheet**

1. General description

The 74HC75 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC75 is specified in compliance with JEDEC standard no. 7A.

The 74HC75 has four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs (LE12 and LE34). When LEnn is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LEnn is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LEnn will be stored in the latches. The latched outputs remain stable as long as the LEnn is LOW.

2. Features

- Complementary Q and $\overline{Q}$ outputs
- V_{CC} and GND on the center pins
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.



3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V					
	nD to nQ, $n\overline{Q}$			-	11	-	ns
	LEnn to nQ, $n\overline{Q}$			-	11	-	ns
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance per latch	V_I = GND to V_{CC}	[1]	-	42	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC75N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC75D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC75DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC75PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

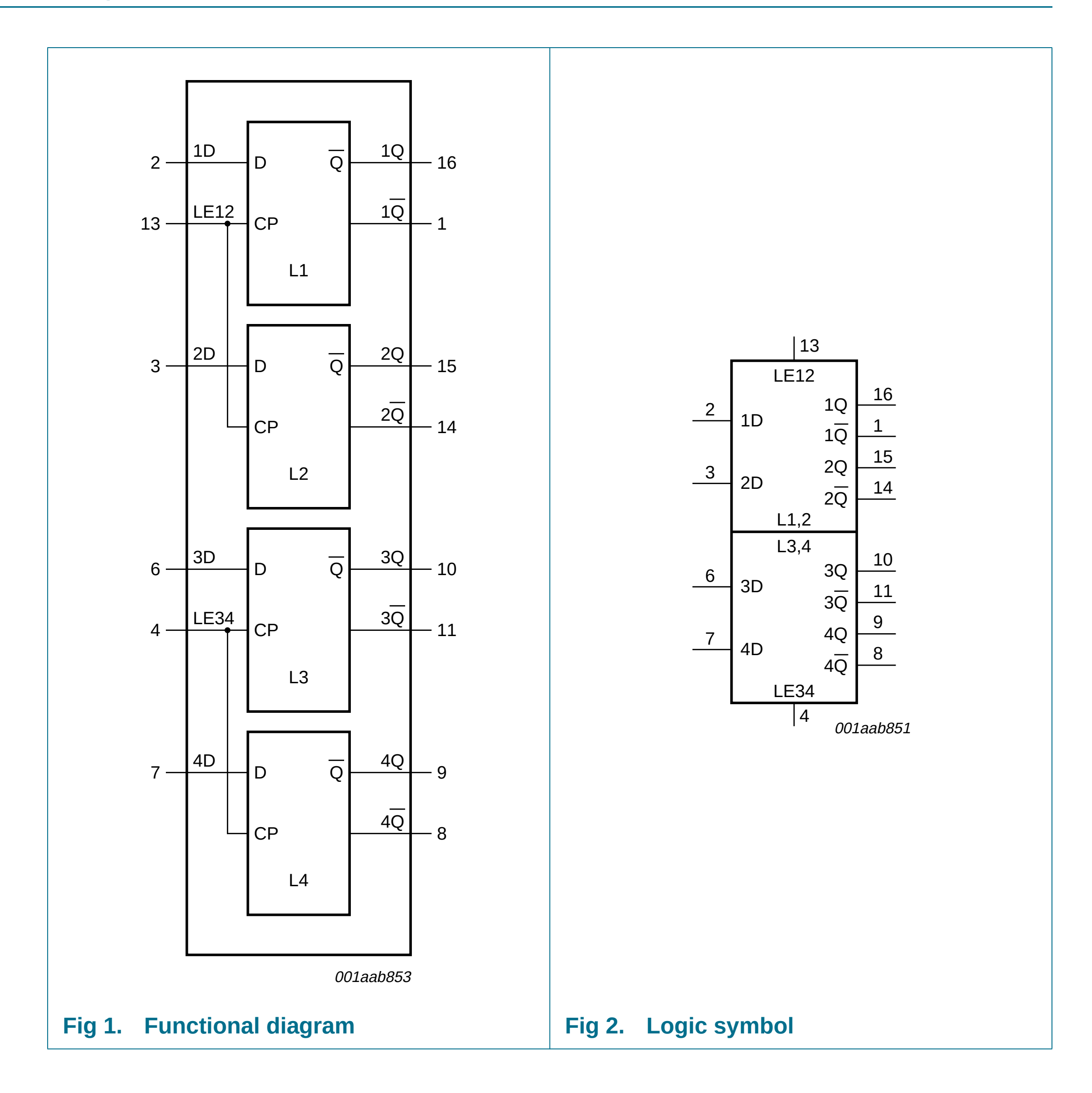


Fig 1. Functional diagram

Fig 2. Logic symbol

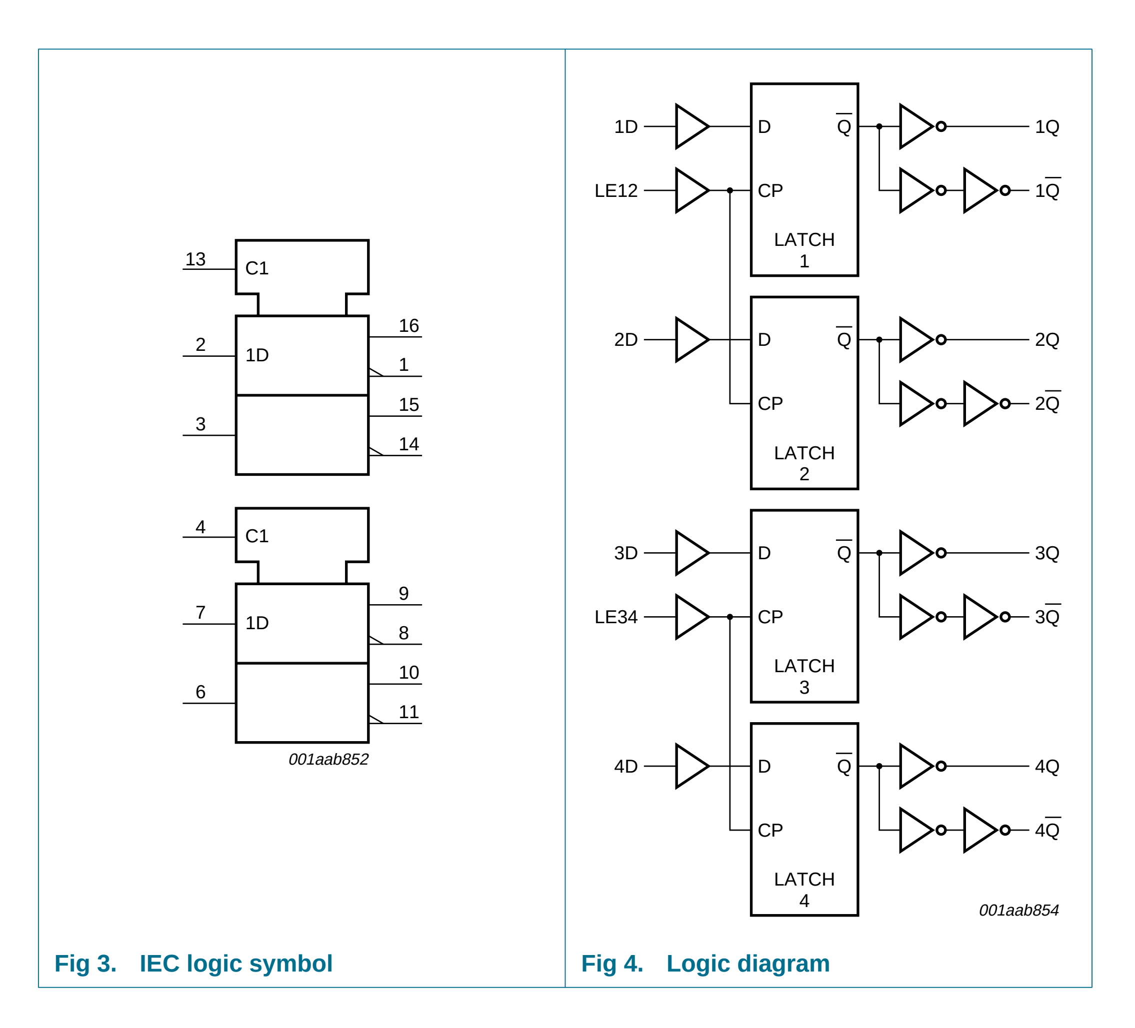


Fig 3. IEC logic symbol

Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

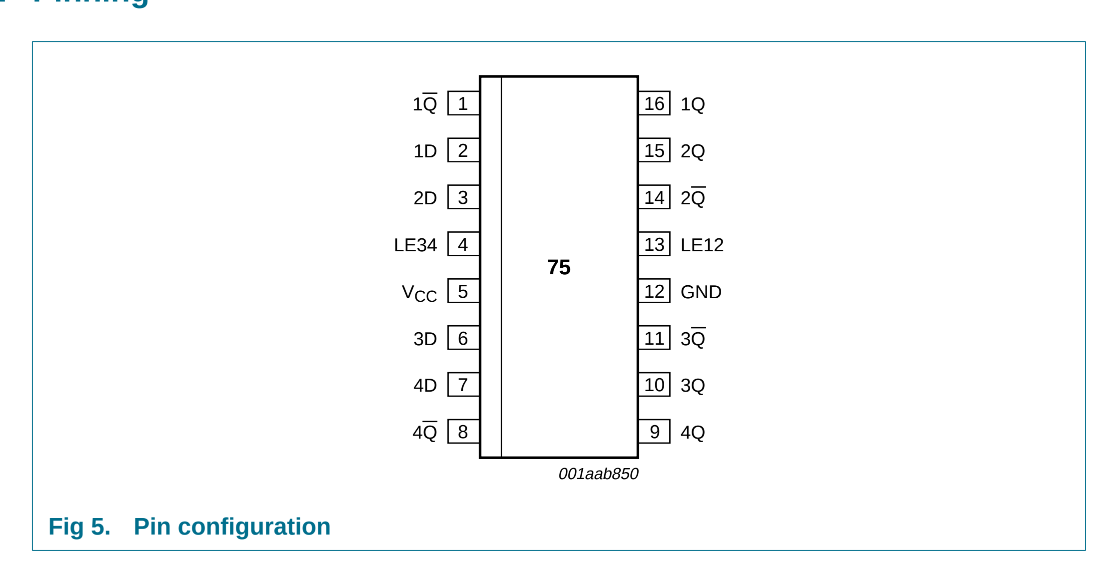


Fig 5. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1$\overline{Q}$	1	complementary latch output 1
1D	2	data input 1
2D	3	data input 2
LE34	4	latch enable input for latches 3 and 4 (active HIGH)
V_{CC}	5	positive supply voltage
3D	6	data input 3
4D	7	data input 4
4$\overline{Q}$	8	complementary latch output 4
4Q	9	latch output 4
3Q	10	latch output 3
3$\overline{Q}$	11	complementary latch output 3
GND	12	ground (0 V)
LE12	13	latch enable input for latches 1 and 2 (active HIGH)
2$\overline{Q}$	14	complementary latch output 2
2Q	15	latch output 2
1Q	16	latch output 1

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input		Output	
	LEnn	nD	nQ	n$\overline{Q}$
Data enabled	H	L	L	H
	H	H	H	L
Data latched	L	X	q	$\overline{q}$

[1] H = HIGH voltage level;
L = LOW voltage level;
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW LEnn transition;
X = don't care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output source or sink current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation					
	DIP16 package		[1]	-	750	mW
	SO16, SSOP16 and TSSOP16 packages		[2]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times	$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
T_{amb}	ambient temperature		–40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

11. Dynamic characteristics

Table 8: Dynamic characteristics
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; unless otherwise specified, see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL}, t_{PLH}	propagation delay nD to nQ	see Figure 6				
		$V_{CC} = 2.0$ V	-	33	110	ns
		$V_{CC} = 4.5$ V	-	12	22	ns
		$V_{CC} = 6.0$ V	-	10	19	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	ns
	propagation delay nD to $n\overline{Q}$	see Figure 7				
		$V_{CC} = 2.0$ V	-	39	120	ns
		$V_{CC} = 4.5$ V	-	14	24	ns
		$V_{CC} = 6.0$ V	-	11	20	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	ns
	propagation delay LEnn to nQ	see Figure 9				
		$V_{CC} = 2.0$ V	-	33	120	ns
		$V_{CC} = 4.5$ V	-	12	24	ns
		$V_{CC} = 6.0$ V	-	10	20	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	ns
	propagation delay LEnn to $n\overline{Q}$	see Figure 9				
		$V_{CC} = 2.0$ V	-	39	125	ns
		$V_{CC} = 4.5$ V	-	14	25	ns
		$V_{CC} = 6.0$ V	-	11	21	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6 and 7				
		$V_{CC} = 2.0$ V	-	19	75	ns
		$V_{CC} = 4.5$ V	-	7	15	ns
		$V_{CC} = 6.0$ V	-	6	13	ns
t_W	enable pulse width HIGH	see Figure 9				
		$V_{CC} = 2.0$ V	80	17	-	ns
		$V_{CC} = 4.5$ V	16	6	-	ns
		$V_{CC} = 6.0$ V	14	5	-	ns
t_{su}	set-up time nD to LEnn	see Figure 8				
		$V_{CC} = 2.0$ V	60	14	-	ns
		$V_{CC} = 4.5$ V	12	5	-	ns
		$V_{CC} = 6.0$ V	10	4	-	ns
t_h	hold time nD to LEnn	see Figure 8				
		$V_{CC} = 2.0$ V	3	–8	-	ns
		$V_{CC} = 4.5$ V	3	–3	-	ns
		$V_{CC} = 6.0$ V	3	–2	-	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; unless otherwise specified, see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{PD}	power dissipation capacitance per latch	V_I = GND to V_{CC} [1]	-	42	-	pF
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay nD to nQ	see Figure 6				
		V_{CC} = 2.0 V	-	-	140	ns
		V_{CC} = 4.5 V	-	-	28	ns
		V_{CC} = 6.0 V	-	-	24	ns
	propagation delay nD to $n\overline{Q}$	see Figure 7				
		V_{CC} = 2.0 V	-	-	150	ns
		V_{CC} = 4.5 V	-	-	30	ns
		V_{CC} = 6.0 V	-	-	26	ns
	propagation delay LEnn to nQ	see Figure 9				
		V_{CC} = 2.0 V	-	-	150	ns
		V_{CC} = 4.5 V	-	-	30	ns
		V_{CC} = 6.0 V	-	-	26	ns
	propagation delay LEnn to $n\overline{Q}$	see Figure 9				
		V_{CC} = 2.0 V	-	-	155	ns
		V_{CC} = 4.5 V	-	-	31	ns
		V_{CC} = 6.0 V	-	-	26	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6 and 7				
		V_{CC} = 2.0 V	-	-	95	ns
		V_{CC} = 4.5 V	-	-	19	ns
		V_{CC} = 6.0 V	-	-	16	ns
t_W	enable pulse width HIGH	see Figure 9				
		V_{CC} = 2.0 V	100	-	-	ns
		V_{CC} = 4.5 V	20	-	-	ns
		V_{CC} = 6.0 V	17	-	-	ns
t_{su}	set-up time nD to LEnn	see Figure 8				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns
t_h	hold time nD to LEnn	see Figure 8				
		V_{CC} = 2.0 V	3	-	-	ns
		V_{CC} = 4.5 V	3	-	-	ns
		V_{CC} = 6.0 V	3	-	-	ns

Table 8: Dynamic characteristics *…continued*

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; unless otherwise specified, see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay nD to nQ	see Figure 6				
		V_{CC} = 2.0 V	-	-	165	ns
		V_{CC} = 4.5 V	-	-	33	ns
		V_{CC} = 6.0 V	-	-	28	ns
	propagation delay nD to $n\overline{Q}$	see Figure 7				
		V_{CC} = 2.0 V	-	-	180	ns
		V_{CC} = 4.5 V	-	-	36	ns
		V_{CC} = 6.0 V	-	-	31	ns
	propagation delay LEnn to nQ	see Figure 9				
		V_{CC} = 2.0 V	-	-	180	ns
		V_{CC} = 4.5 V	-	-	36	ns
		V_{CC} = 6.0 V	-	-	31	ns
	propagation delay LEnn to $n\overline{Q}$	see Figure 9				
		V_{CC} = 2.0 V	-	-	190	ns
		V_{CC} = 4.5 V	-	-	38	ns
		V_{CC} = 6.0 V	-	-	32	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6 and 7				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	enable pulse width HIGH	see Figure 9				
		V_{CC} = 2.0 V	120	-	-	ns
		V_{CC} = 4.5 V	24	-	-	ns
		V_{CC} = 6.0 V	20	-	-	ns
t_{su}	set-up time nD to LEnn	see Figure 8				
		V_{CC} = 2.0 V	90	-	-	ns
		V_{CC} = 4.5 V	18	-	-	ns
		V_{CC} = 6.0 V	15	-	-	ns
t_h	hold time nD to LEnn	see Figure 8				
		V_{CC} = 2.0 V	3	-	-	ns
		V_{CC} = 4.5 V	3	-	-	ns
		V_{CC} = 6.0 V	3	-	-	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

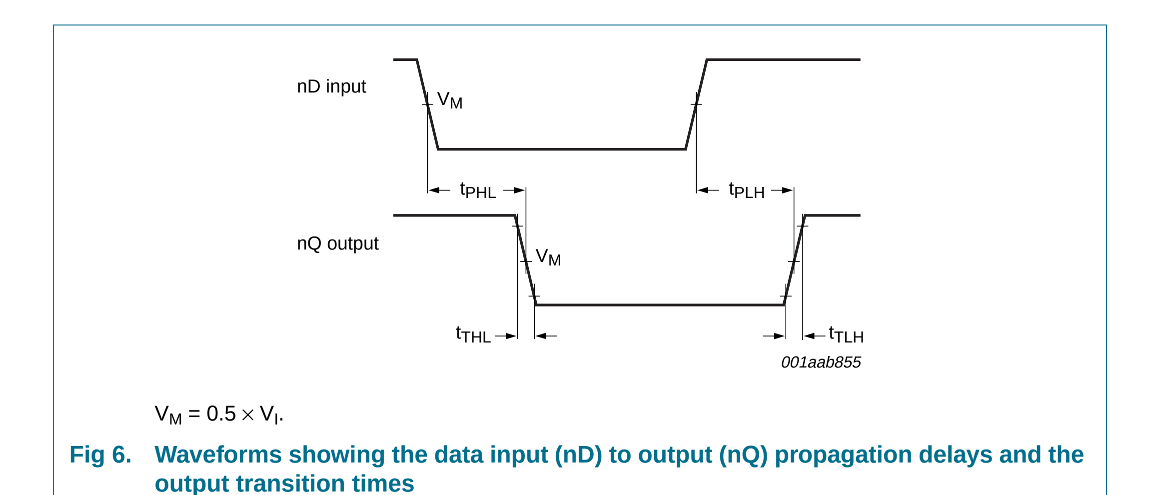
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

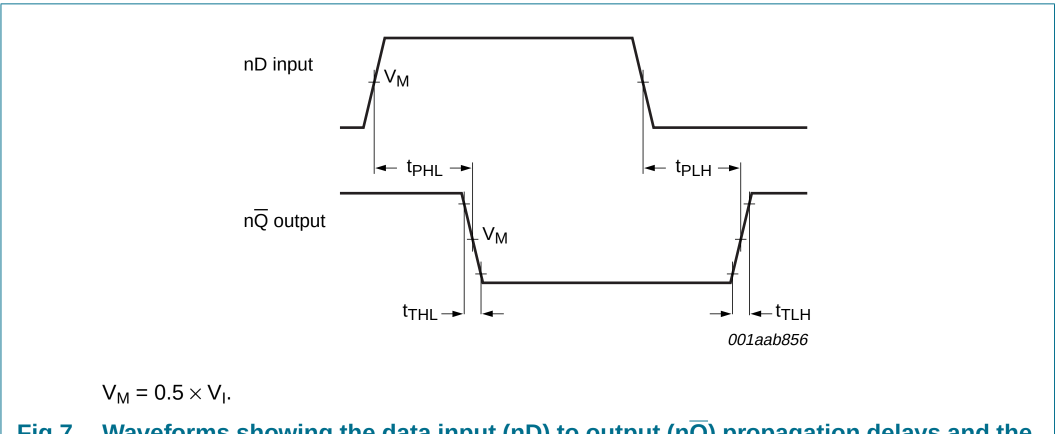
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



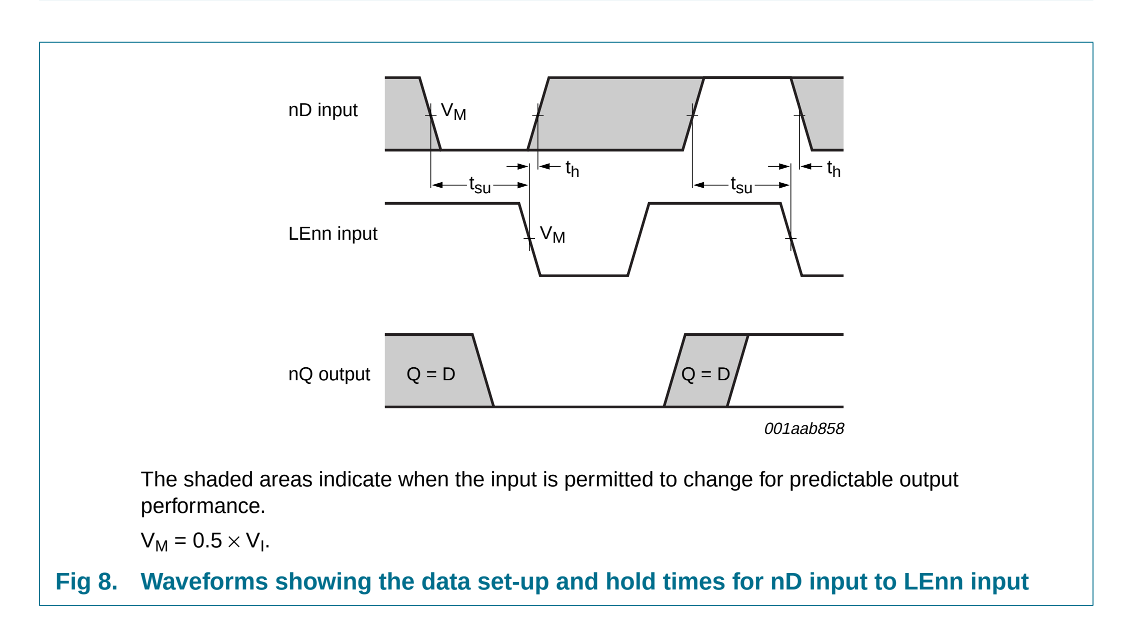
$V_M = 0.5 \times V_I$.

Fig 6. Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times



$V_M = 0.5 \times V_I$.

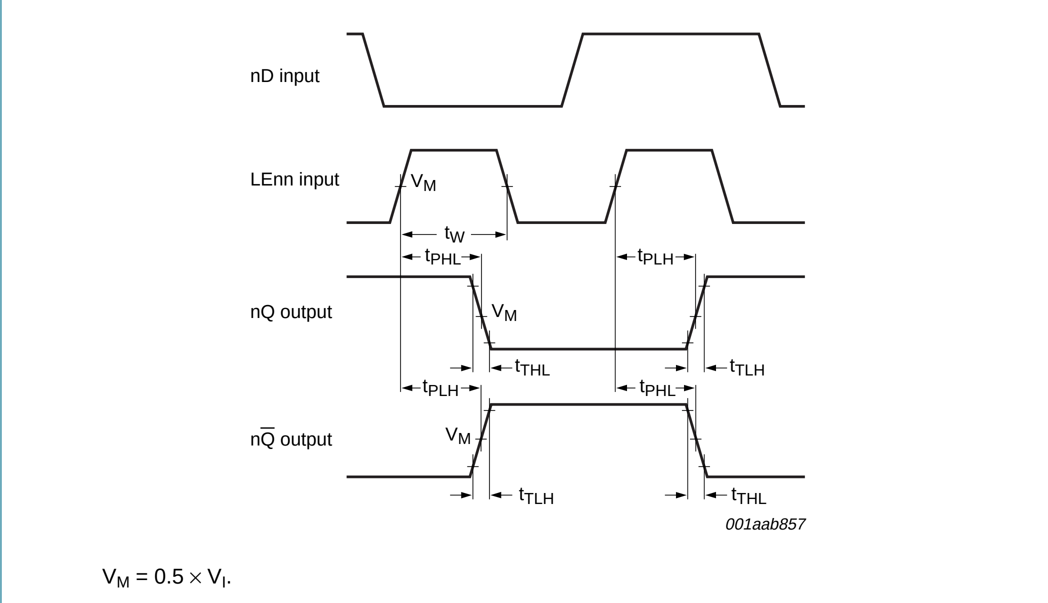
Fig 7. Waveforms showing the data input (nD) to output ($n\overline{Q}$) propagation delays and the output transition times



The shaded areas indicate when the input is permitted to change for predictable output performance.

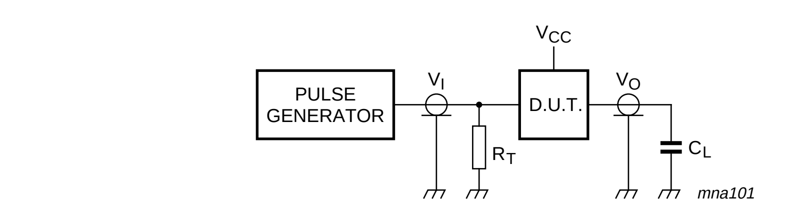
$V_M = 0.5 \times V_I$.

Fig 8. Waveforms showing the data set-up and hold times for nD input to LEnn input



$V_M = 0.5 \times V_I$.

Fig 9. Waveforms showing the latch enable input (LEnn) pulse width, the latch enable input to outputs (nQ, n$\overline{Q}$) propagation delays and the output transition times



Test data is given in Table 9.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

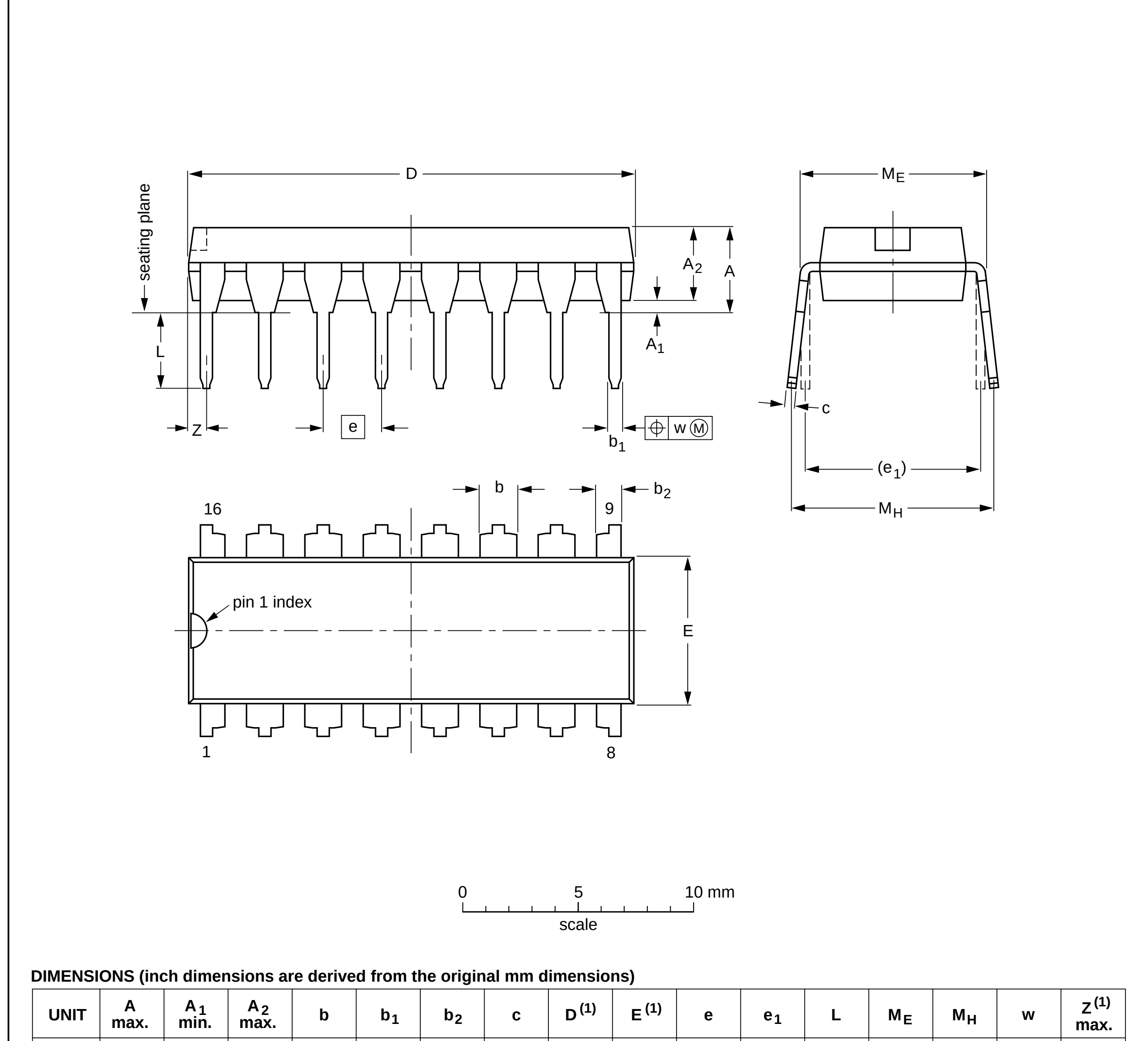
Fig 10. Load circuitry for switching times

Table 9: Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

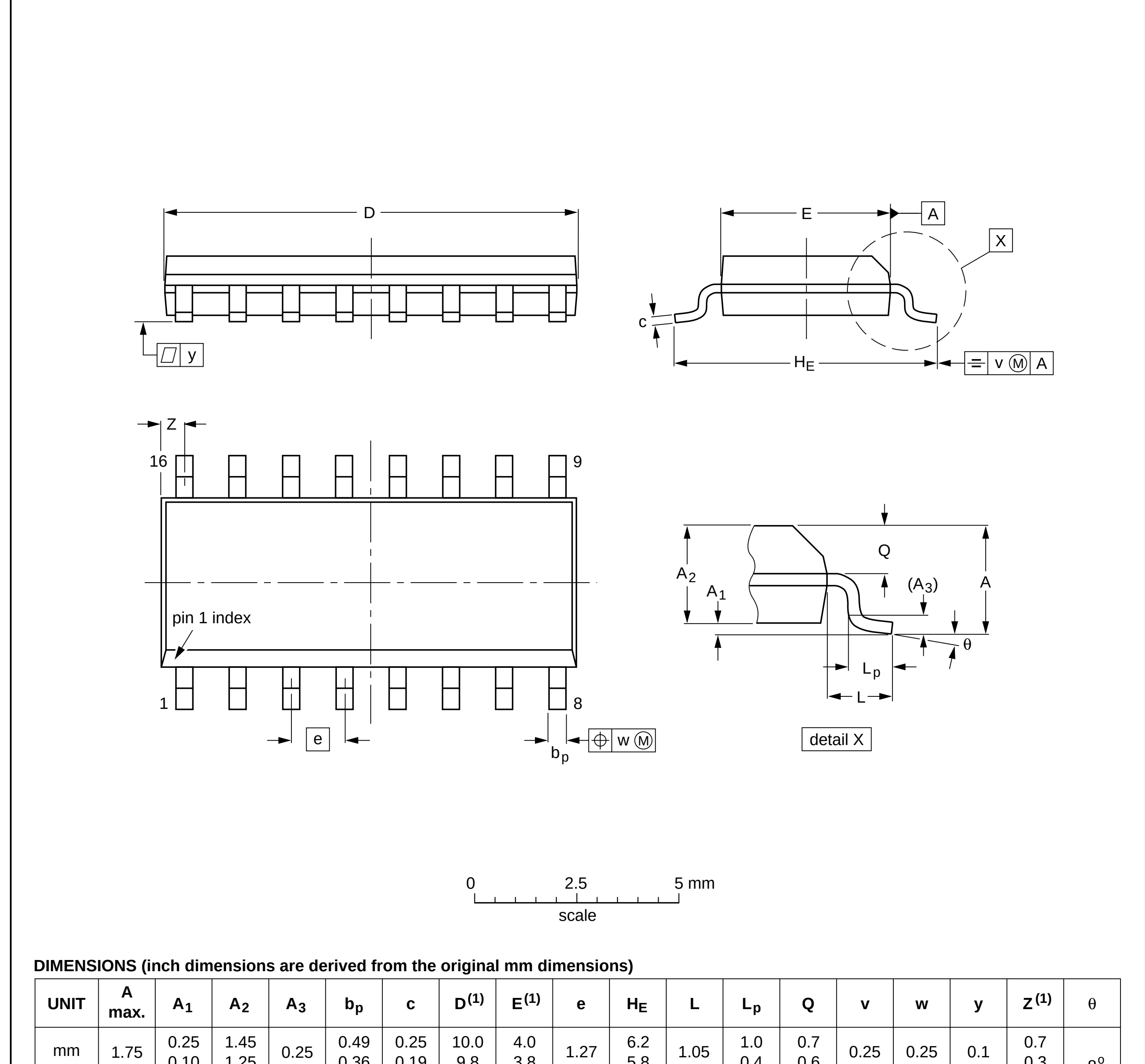
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 11. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

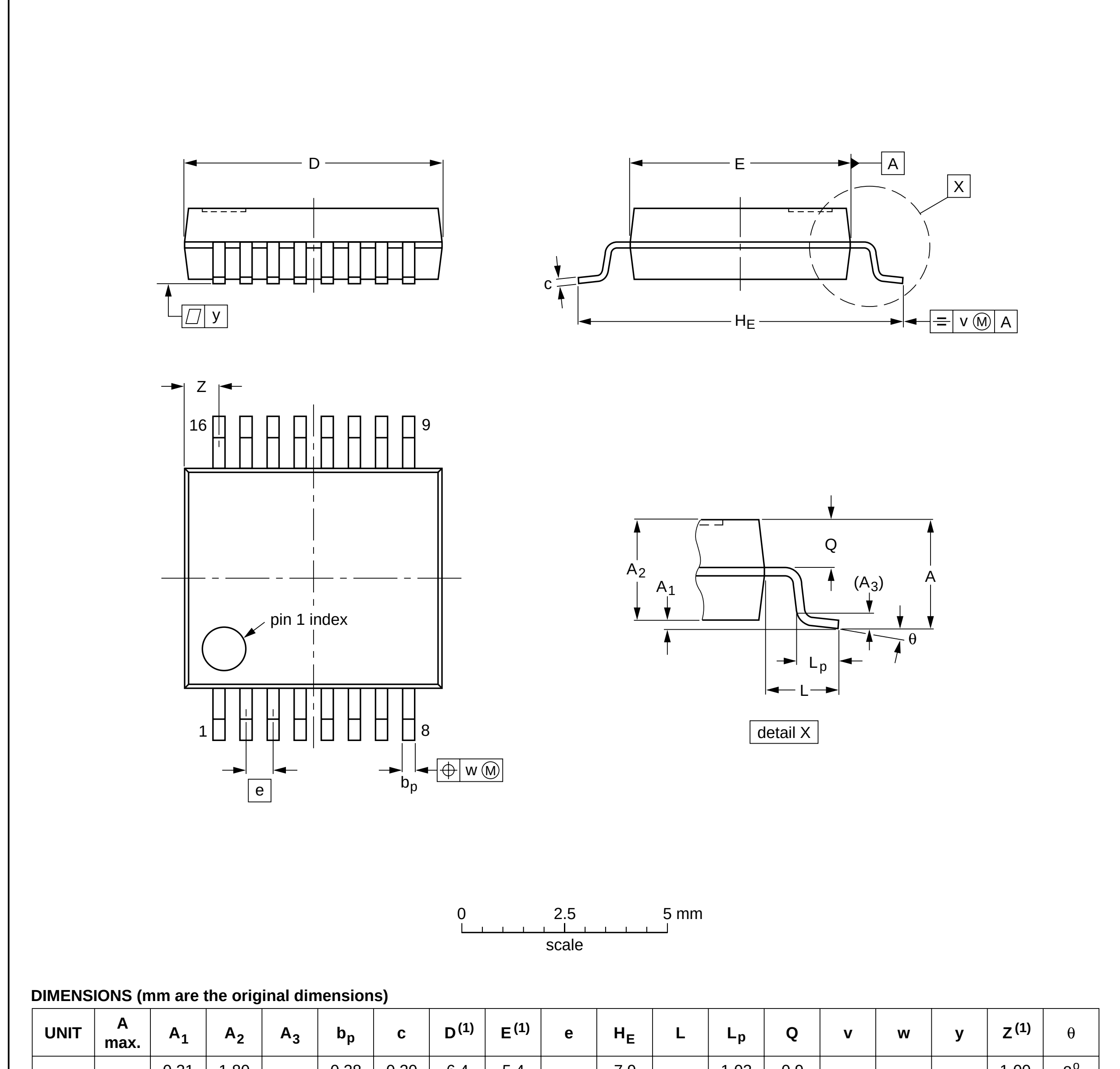
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

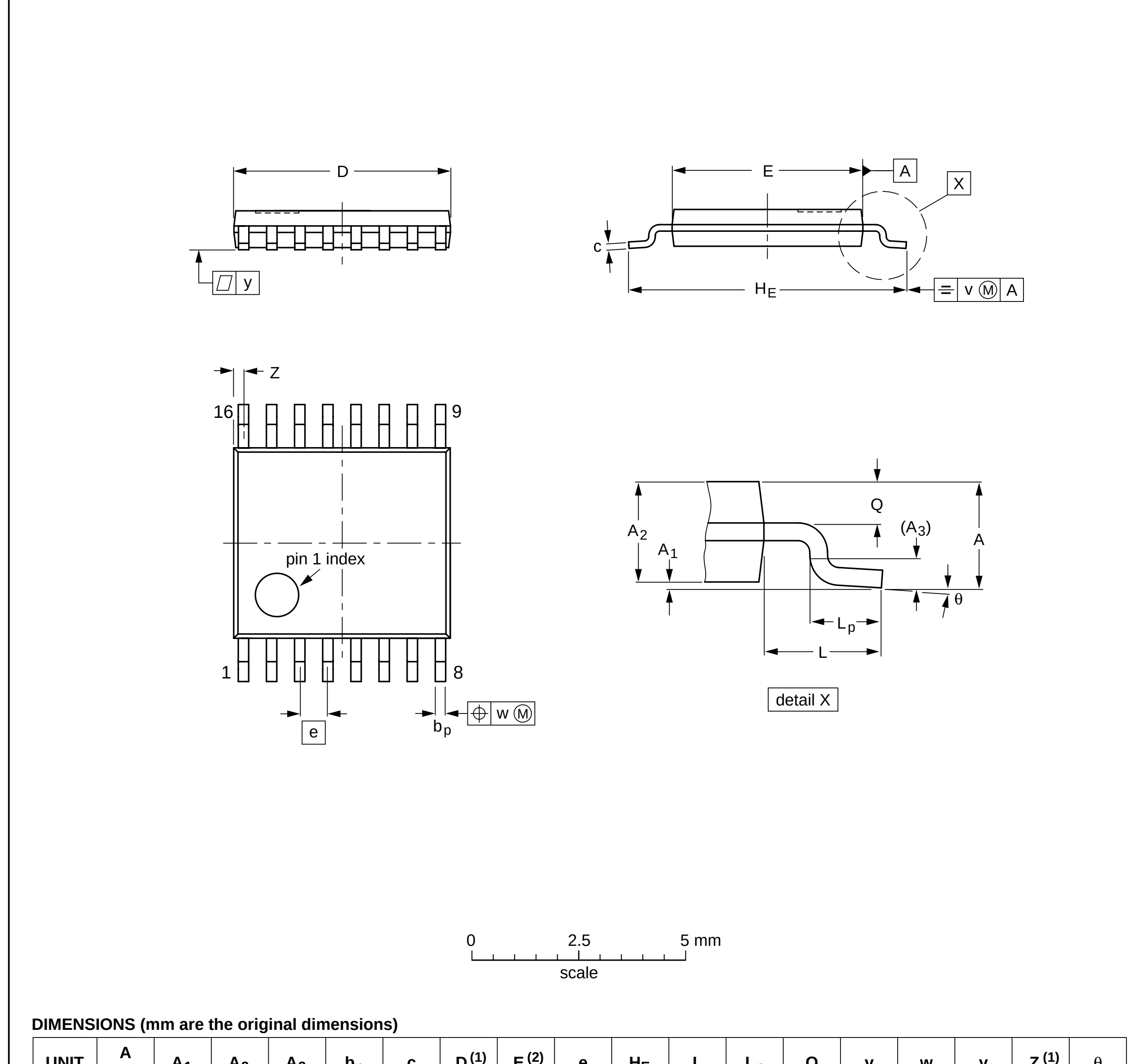
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT403-1 (TSSOP16)

14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC75_3	20041112	Product data sheet	-	9397 750 13816	74HC_HCT75_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT75. • Inserted family specification.				
74HC_HCT75_CNV_2	19970918	Product specification	-	-	74HC_HCT75_1
74HC_HCT75_1	19901201	Product specification	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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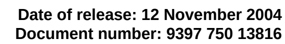
18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

19. Contents




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